REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated October 8, 1999 have been carefully reviewed by the Applicants. In response, Applicants have amended the claims. Applicants respectfully request the Examiner to consider and allow the amended claims.

Claims 1-14 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Accordingly, Applicants have amended these claims to more particularly and distinctly claim the present invention.

Claims 10 and 12-14 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hathaway et al. (U.S. Patent No. 5,757,657). The Hathaway reference pertains to an adaptive incremental placement process of circuits on a VLSI chip. More specifically, Hathaway relates to a computer implemented method that incrementally updates a design placement in a VLSI chip.

In contrast, independent Claim 10 has been amended to include the limitation of a rough placement logic for placing cells of an integrated circuit design represented as a netlist having cells and connections between the cells. The rough placement logic comprises a cell separator, a synthesis too, a partitioner, a spacer, and a comparator. It is respectfully submitted that Hathaway does not teach, disclose, suggest, or render obvious a rough placement logic as claimed in the present invention.

not how claim language reads

↑ the argument — it's just semantics

Claims 1-3 and 5-9 stand rejected under 35 U.S.C. §103(a) as being obvious over Hathaway in view of Cheng (U.S. Patent No. 5,847,965), or Jones et al. (U.S. Patent No. 5,629,860), or Modarres et al. (U.S. Patent No. 4,918,614). As discussed above, the Hathaway reference pertains to an adaptive incremental placement process of circuits on a VLSI chip. The Cheng reference pertains to a method for automatic iterative area placement of module cells in an integrated circuit layout. The Jones reference pertains to a method for determining timing delays associated with placement and routing of an integrated circuit. And the Modarres reference pertains to a hierarchical floorplanner.

In contrast, the present invention pertains to a method and apparatus for a rough placement process which is adaptive to netlist changes. Accordingly, Applicants have amended independent Claims 1 and 10 to add the limitation whereby the netlist changes are made during the rough placement process. The significance of the present invention is that by allowing netlist changes to be entered during the rough placement process, the overall number of iterations required for the design of the integrated circuits is minimized. Applicants respectfully submit that neither Hathaway, Cheng, Jones, or Modarres either separately or combined teach, disclose, suggest, or render obvious the present invention of modifying the netlist during the rough placement process.

Therefore, it is respectfully submitted that all claims are now in condition for allowance and such action is earnestly solicited by the Applicants.

If there are any additional charges, please charge them to our Deposit Account Number 23-0085.

Respectfully submitted,

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